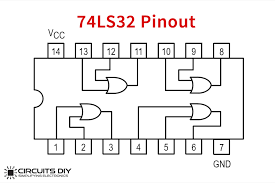
DLD LAB Exam

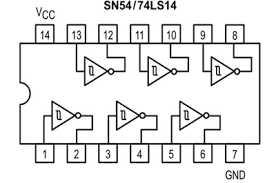
**2-Input OR Gate Implementation:**

IC Name: 74LS32



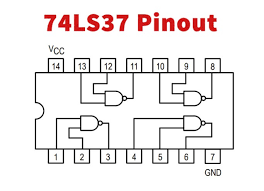
**NOT Gate Implementation:**

IC Name: G-74LS15



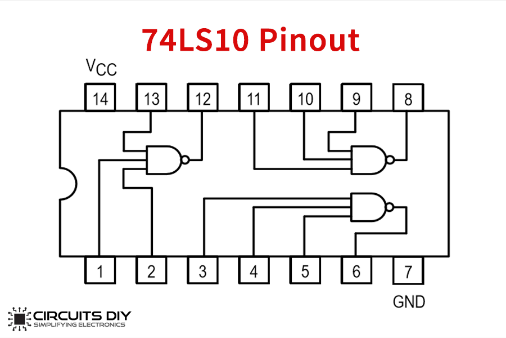
**2-Input NAND Gate Implementation:**

IC Name: -74LS37



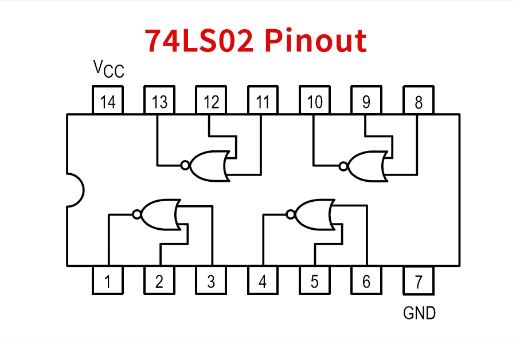
**3-Input NAND Gate:**

IC Name: 74LS10



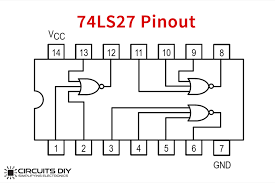
**2-Input NOR Gate:**

IC Name: 74LS02



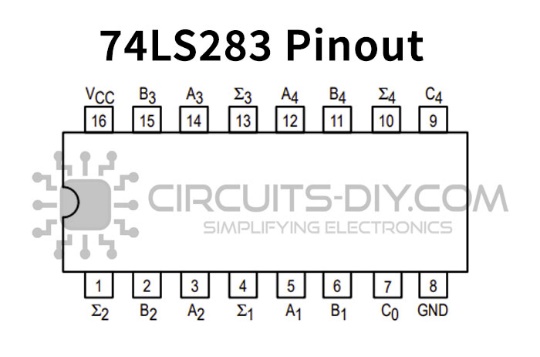
**3-Input NOR Gate Implementation:**

IC Name: 74LS27P



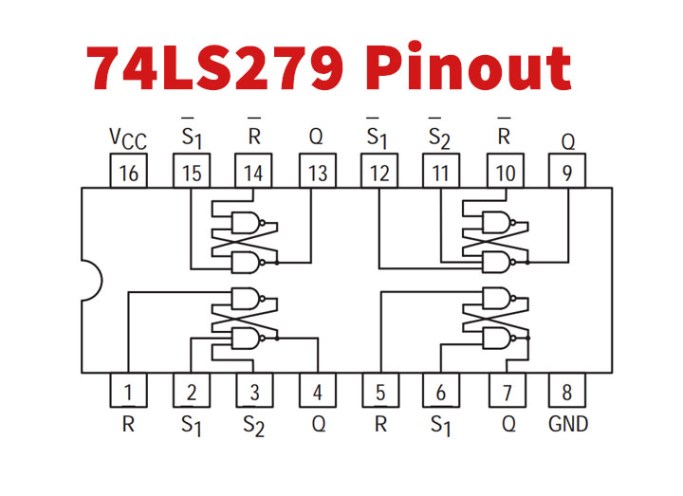
**Full Adder Implementation:**

IC Name: 74LS283



**S-R Latch Implementation:**

IC Name: 74LS279



**Wish You Good Luck**